5th International Workshop on
Crystalline Silicon Solar Cells
Boston, USA - Nov. 1-3, 2011

Mono-crystalline silicon wafers manufactured by casting methods: Optoelectronic, structural and solar cell study

DC WAFERS

UVa

UNIVERSIDAD AUTONOMA DE MADRID

POLITÉCNICA
Instituto de Energía Solar

I. Guerrero, V. Parra, T. Carballo, M. Miranda
B. Moralejo, O. Martínez, J. Jiménez
A. Piñeiro, E. Diéguez
J. F. Lelièvre, C. del Cañizo

Outline

1) Introduction

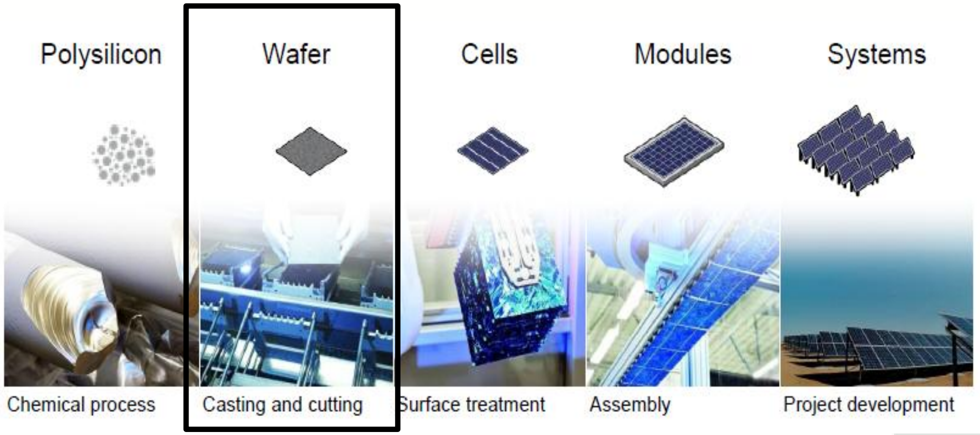
2) The Quasi-mono, pseudo-mono, mono-like ERA.

3) Manufacturing mono-cast ingots: COST (seed recycling)

4) Summary and findings

5) Current status at DCWafers

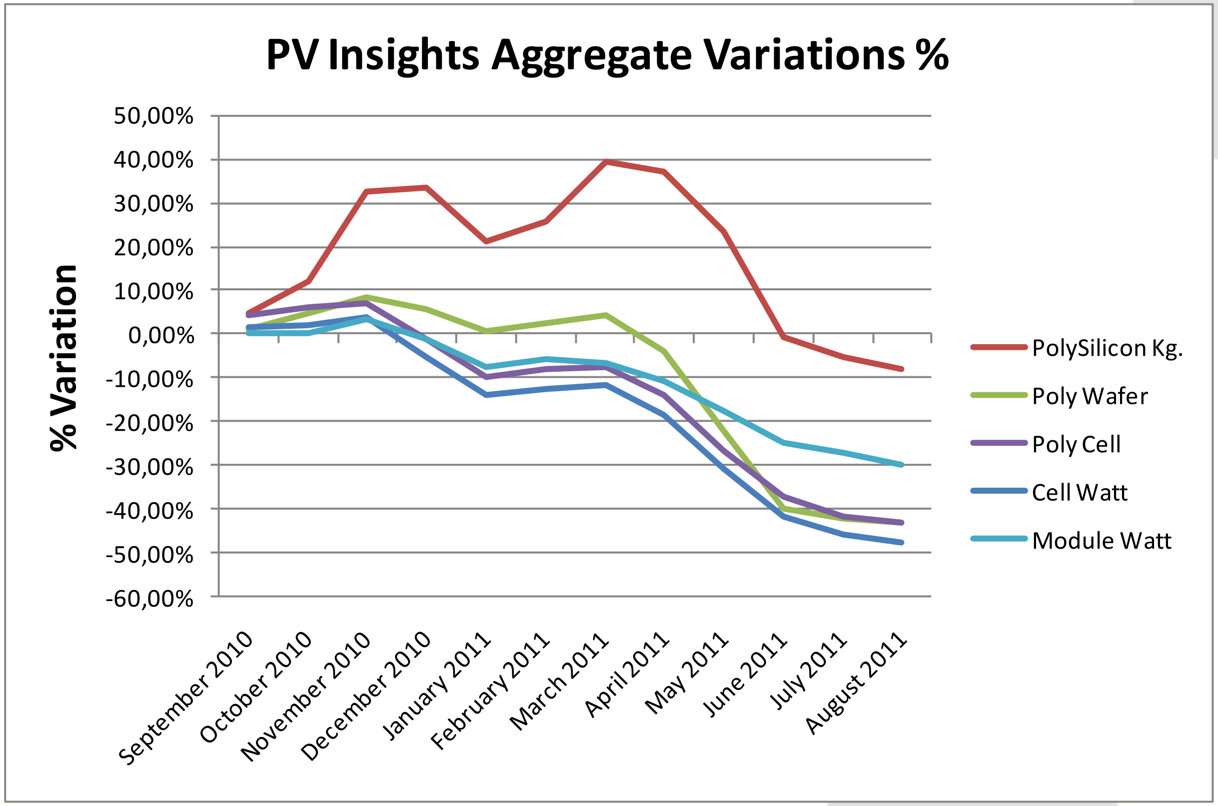
Introduction to DC Wafers Investments, S.L.



- Multicrystaline wafers manufacturer
- Production capacity: 80 MW (1,6 mill./mo.)
- High quality standards

iguerrero@dcwafers.com
vparra@dcwafers.com

PV market evolution



Some facts…

- Up to 50% price decrease (Aug 10'- Aug 11')

3.66 USD/wafer (March 10')
1.53 USD/wafer (October 11')

1.21 USD/Wp (March 10')
0.58 USD/Wp (October 11')

Restricted market: only high efficiency materials and devices are demanded

mc-Si wafer devaluation

Quasi-mono, pseudo-mono, mono-like…

bp solar

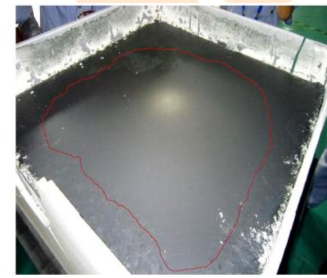
Casting Single Crystal Silicon: Novel Defect Profiles from BP Solar's Mono[2] ™ Wafers

Nathan Stoddard[1, a], Bei Wu[1], Ian Witting[2], Magnus Wagener[2], Yongkook Park[2], George Rozgonyi[2] and Roger Clark[1]

JA SOLAR

MAPLE

PV Production Equipment Conference, 14th April 2011



Jan 11'

ReneSola claims new multi-crystalline wafer comparable in performance to mono

PVTECH

Jul 11'

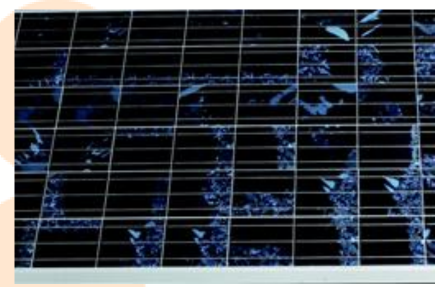
Suntech Unveils Pluto and Mono/Multi Hybrid Modules

greentechsolar

Oct 11'

GCL-Poly building major position in emerging 'quasi-mono' wafer market

PVTECH



GT ADVANCED TECHNOLOGIES

GT Advanced Technologies Announces Commencement of DSS MonoCast(TM) Beta Shipments and Production Testing Partnership with Korean PV Manufacturer Nexolon

Quasi-mono, pseudo-mono, mono-like…

Fundamentals…

Conventional Mono

Rotating pulling
Seed used

Conventional Multi

Gradient directional
Solidification of large Ingot

Mono/Multi crystalline Ingot

**Combination of
Solidification of large Ingots
and
Usage of Seed**

Expected features…

- Lower LID than Cz-Si wafers.
- High efficiency due to Isc boost.
- High productivity as DSS/HEM methods are used lowering **cost** per watt.
- Lower breakage

Usage of Directional Solidification (DSS) and Heat Exchange Method (HEM) furnaces

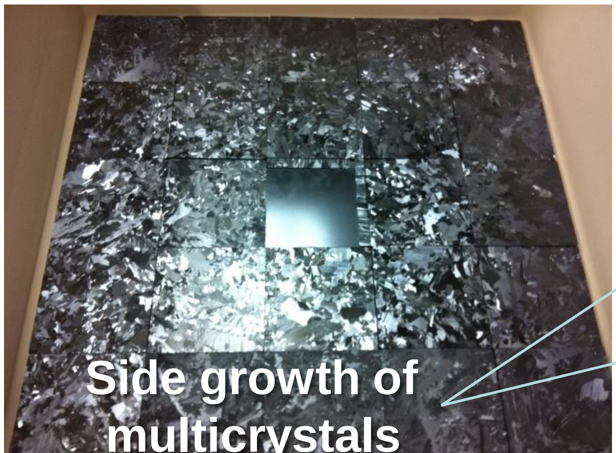
Usage of seeds based on <100> orientated Cz-Si, preferably non-doped. Geometry and size-controlled

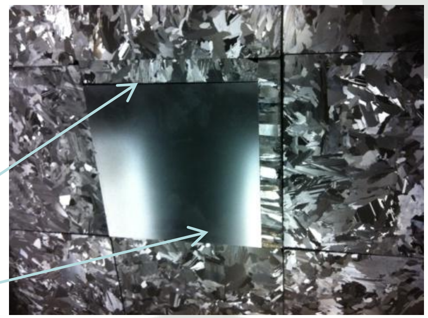
Controlled melting of the seed by thermal engineering (using both software and hardware approaches)

Optimization of the growth speed and temperature control during growth and annealing/cooling processes.

Manufacturing mono-cast ingots

Initial tests at DC Wafers (2010): general behavior of the mono seed



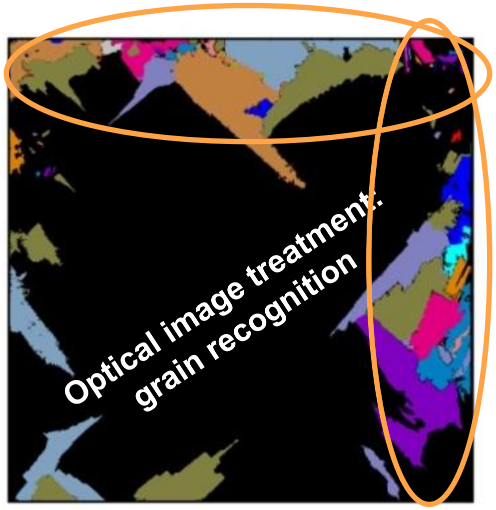


Average values:
EFF = 16.83 %
Isc = 8.53 A
Voc = 623 mV
FF= 77.14%

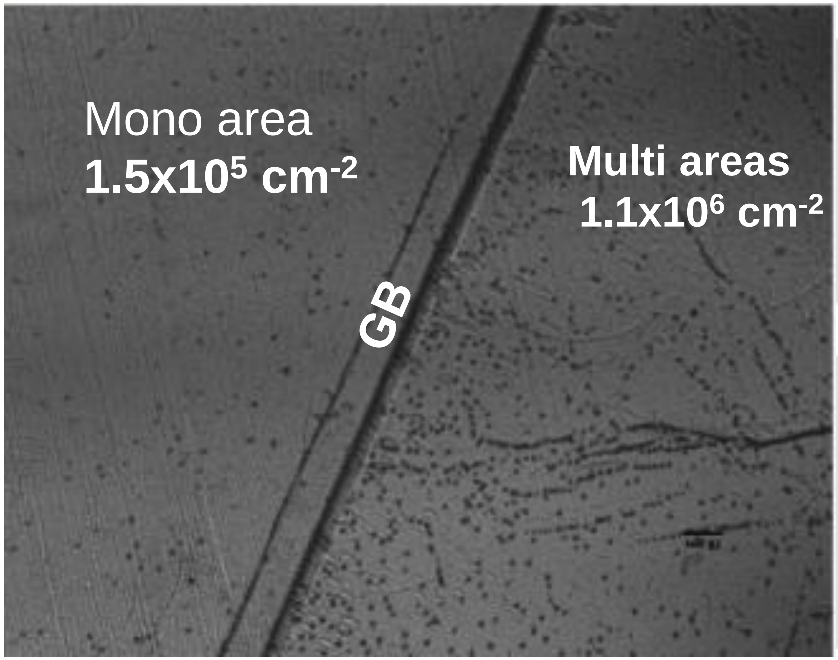
Average values:
EFF = 17.16 %
Isc = 8.55 A
Voc = 628 mV
FF= 77.78%

Central brick
99% (100) monocrystalline

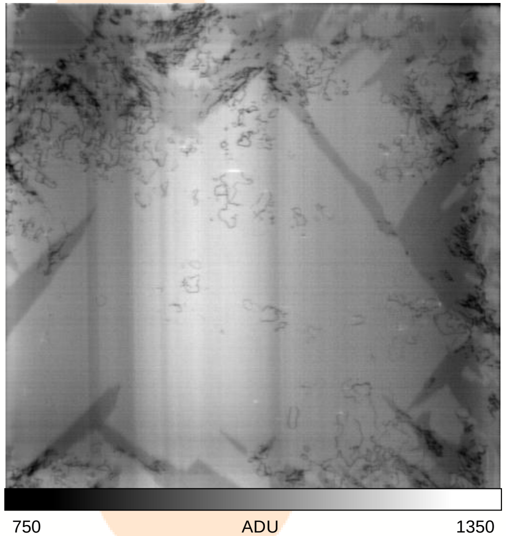
Massive Volume Manufacturing



Etch pit density (EPD) analysis



PL image of an as-cut wafer*



** In collaboration with Semilab*

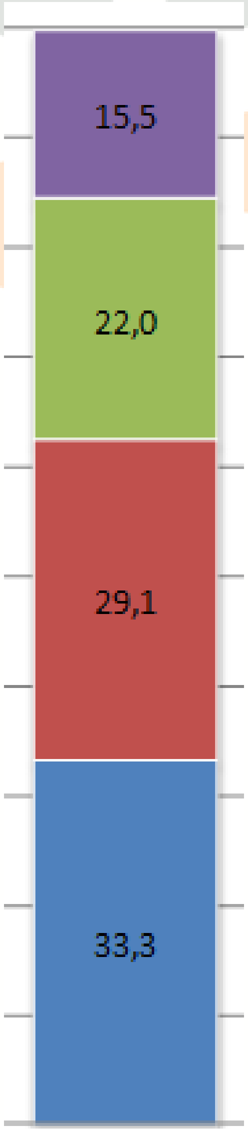
Our clasification

Mono casting (MC)
Monocrystalline 100%

Quasi-mono (QM)
Monocrystalline >90%

DCWafers plus (DCW+)
Monocrystalline >75%

Mc-Si (multi o mono/multi)
Monocrystalline <75%

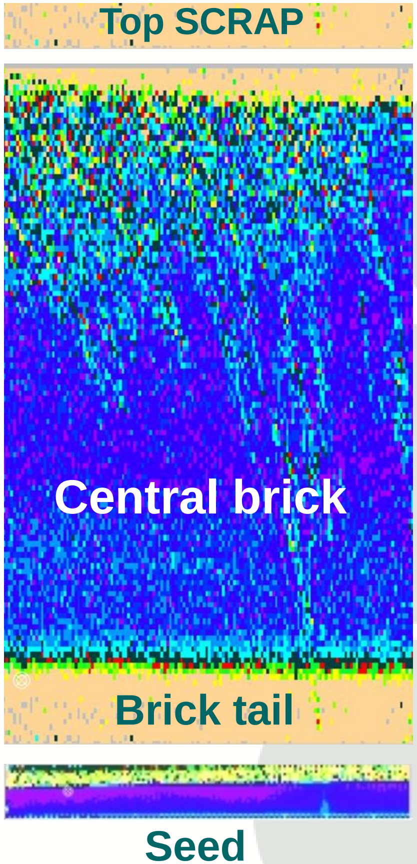


Manufacturing mono-cast ingots: COST

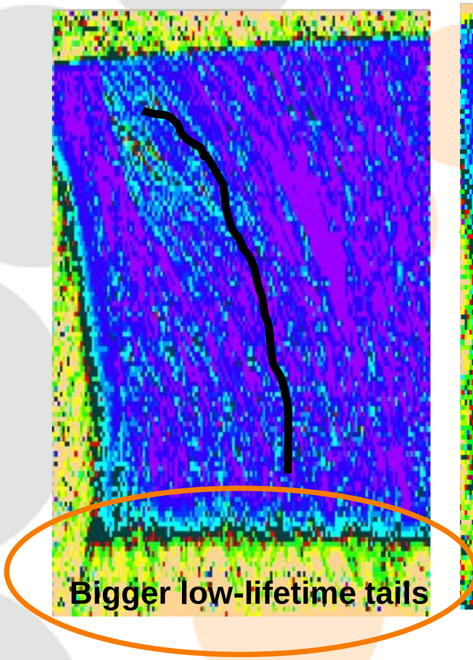
Typical uPCD lifetime behavior at brick level

COST ISSUES
- Bigger tails
- Seed cost
- Cycle time

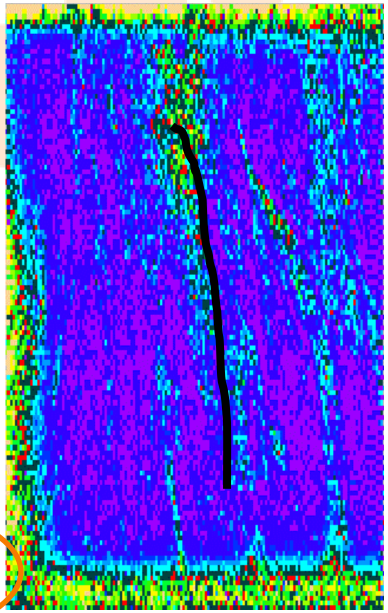
QUALITY ISSUES
- Cell efficiency distribution
- ThermalStress



Seeded growth

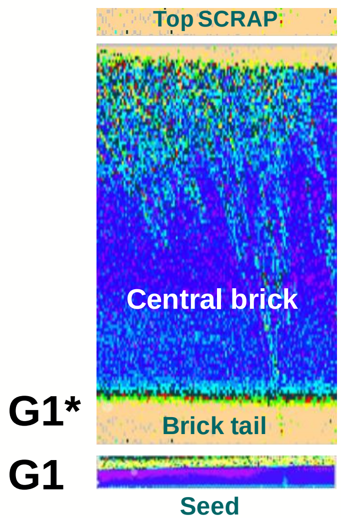


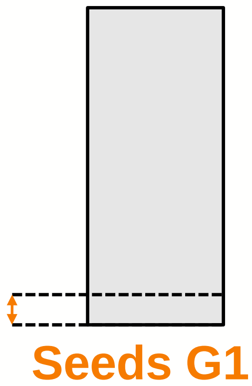
Conventional growth

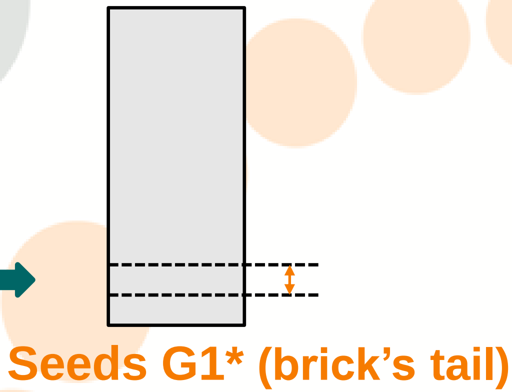


Thermal gradients induce higher growth front curvature when using the seed-assisted approach

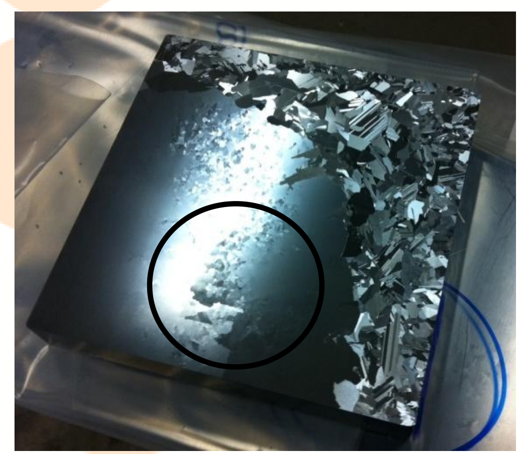
Manufacturing mono-cast ingots







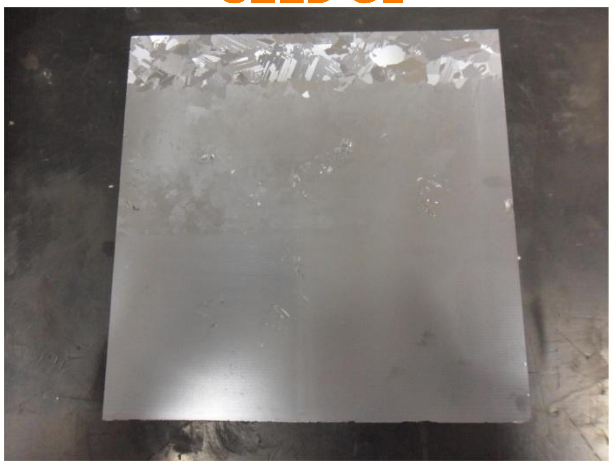
Recycled seeds (Generation n): High-defect regions (sub-grain sGB boundaries)



Manufacturing mono-cast ingots

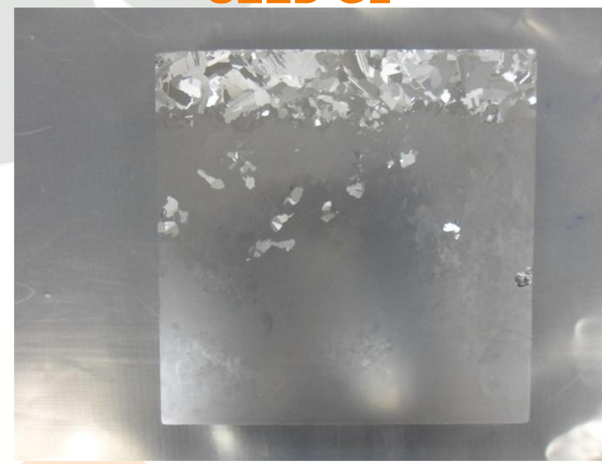
side

SEED G1 | **SEED G2** | **SEED G1***



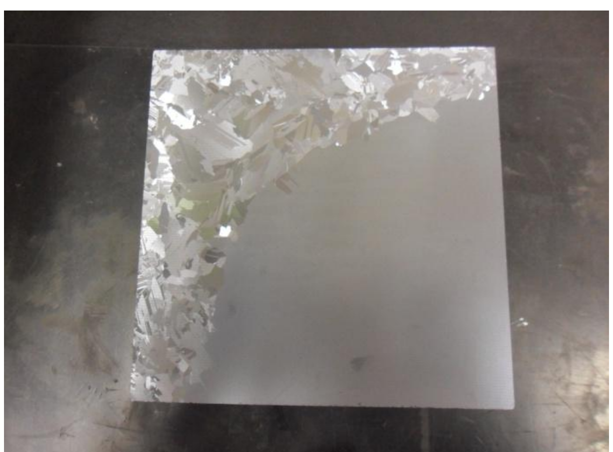
<

<

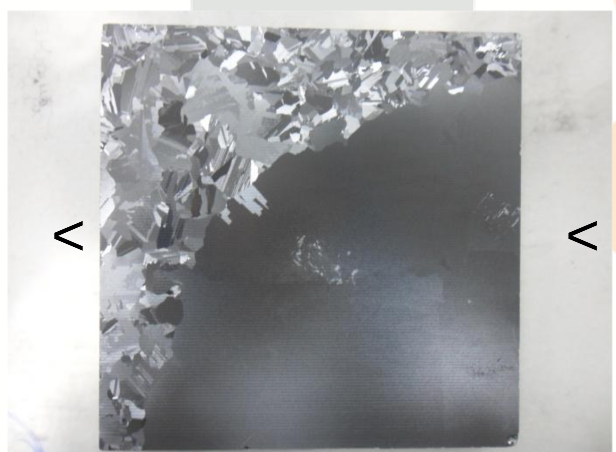


corner

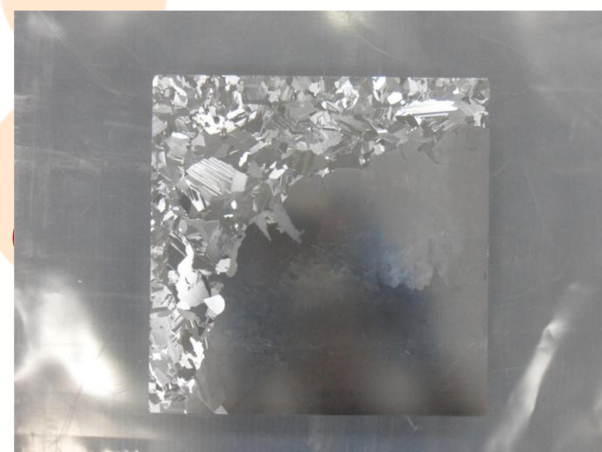
Larger defect areas but higher efficiency



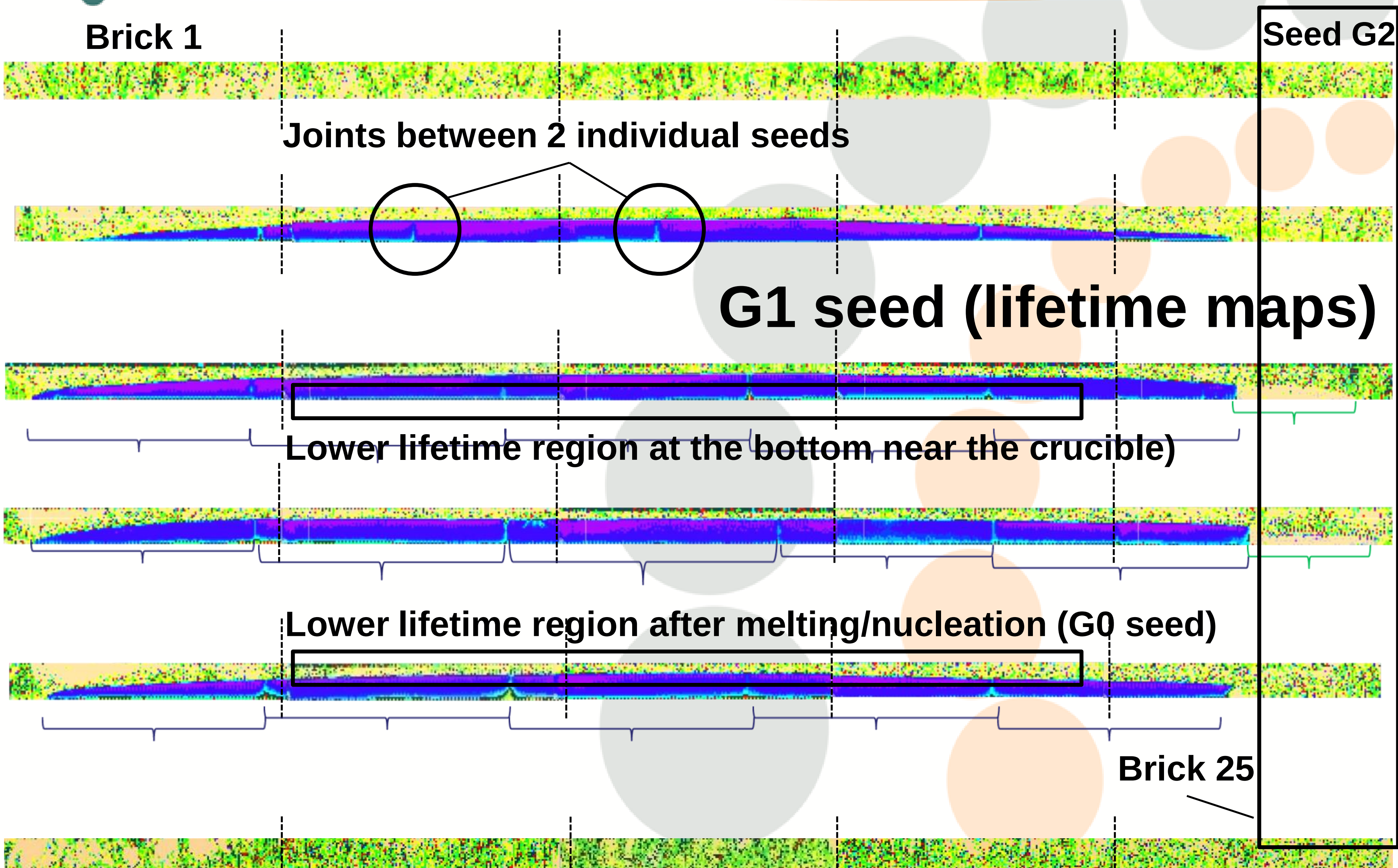
<



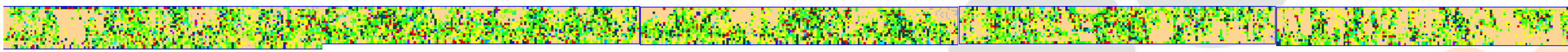
<



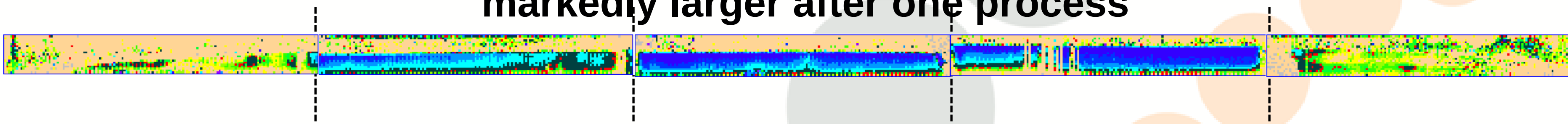
Manufacturing mono-cast ingots



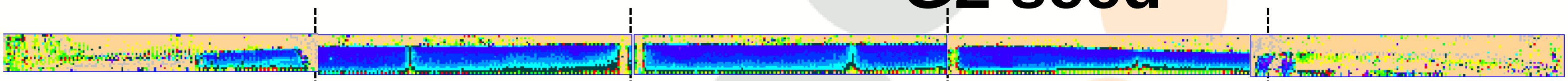
Manufacturing mono-cast ingots



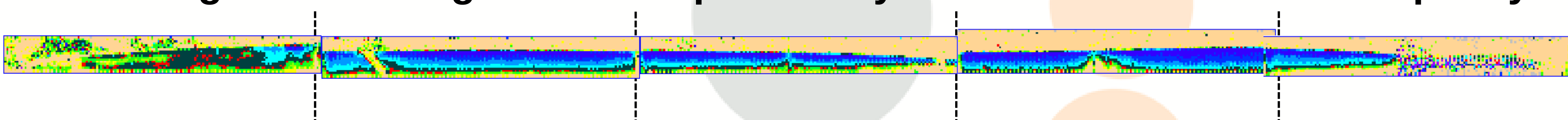
All the previously detected low lifetime regions vs G1-seed are markedly larger after one process

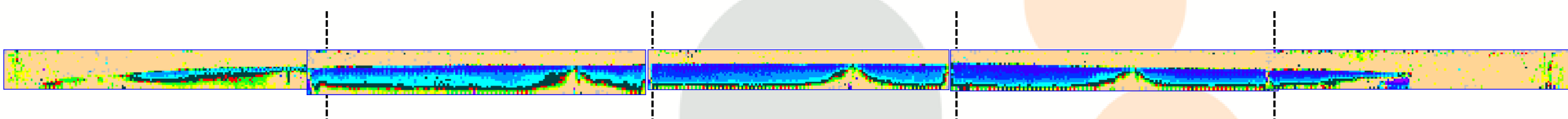


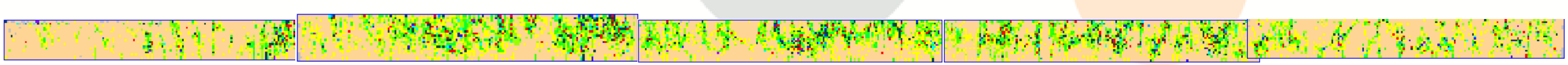
G2 seed



The high lifetime regions of the previously used seed have now lost quality







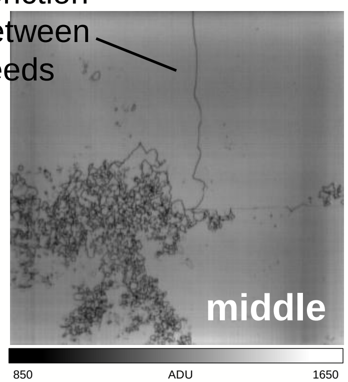
Manufacturing mono-cast ingots

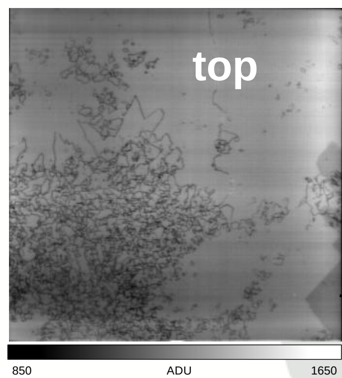
Generation 2-based seeds

- **No MC (100% mono)** wafers after Generation 1
- Visible **defect structures** after KOH/HCl etching of the seeds.
- Lower average efficiency: **<u>Isc</u> as the most contributing factor to decrease efficiency**

G0 wafers (same brick)

Jonction between seeds

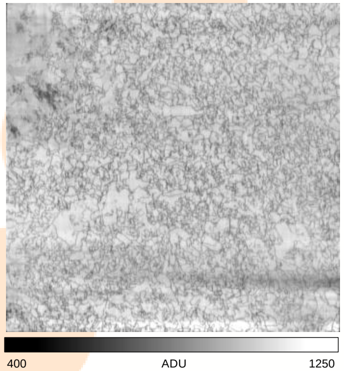




New crystal

Seed recycling

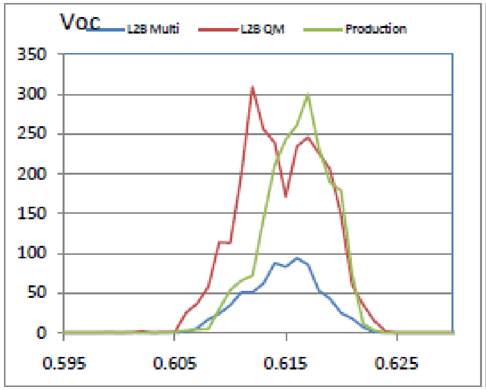
Gn wafers

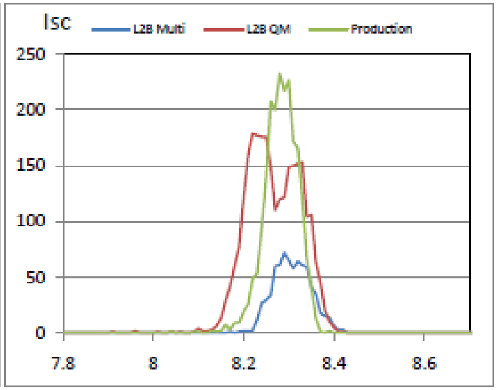


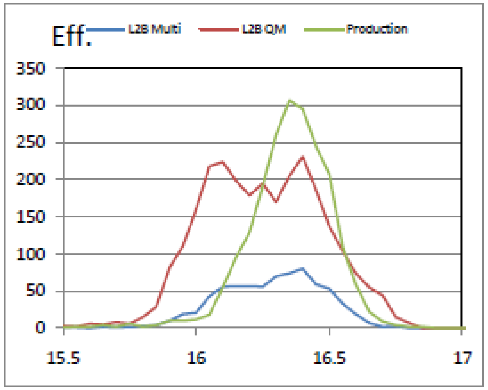
Isc and efficiency related to bulk defect density

Photoluminiscence analysis in collaboration with SEMILAB

<u>QM</u>: Eff = 16.27%
<u>Multi region</u>: Eff = 16.29 %
Reference: Eff = 16.37%



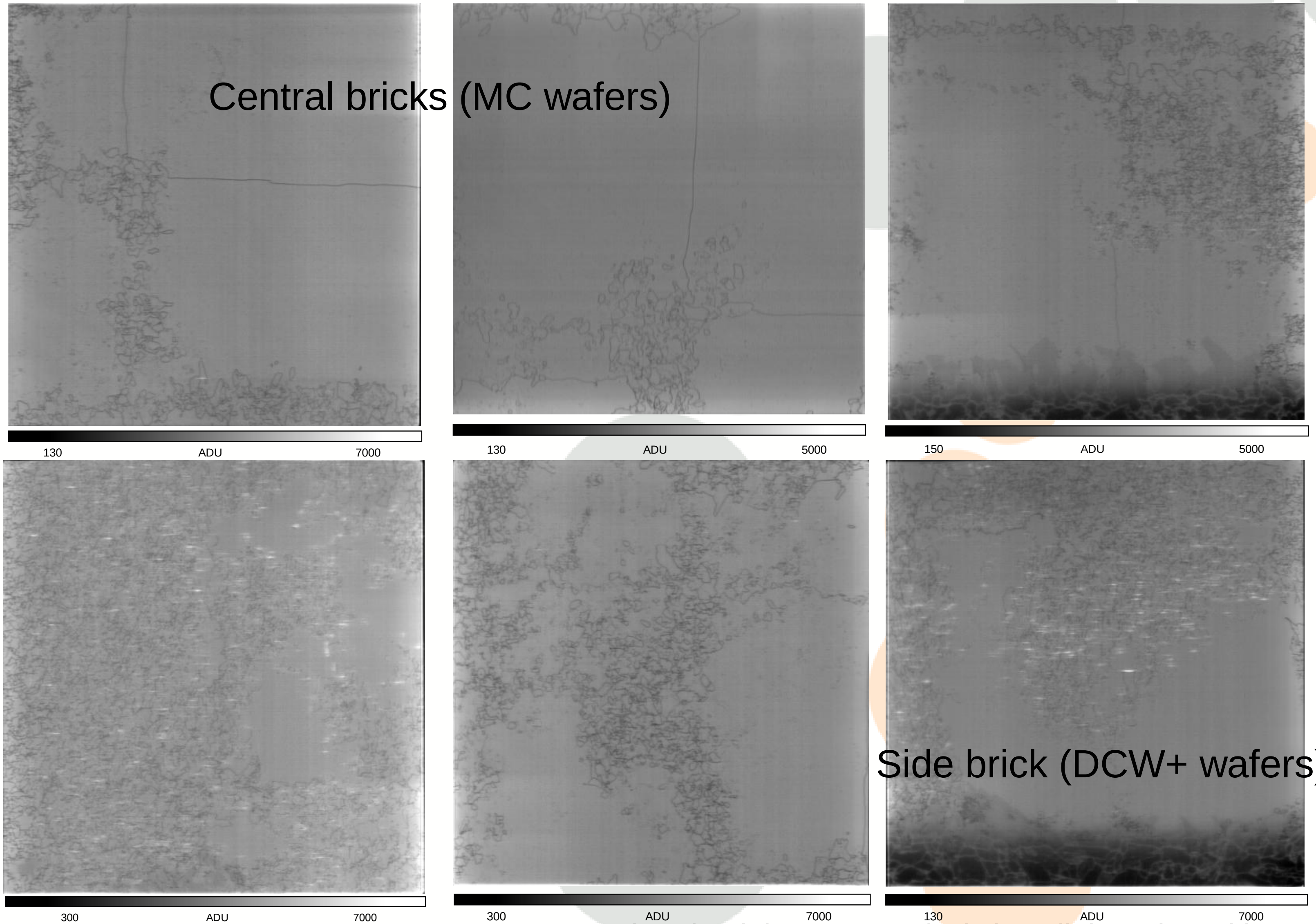




Manufacturing mono-cast ingots

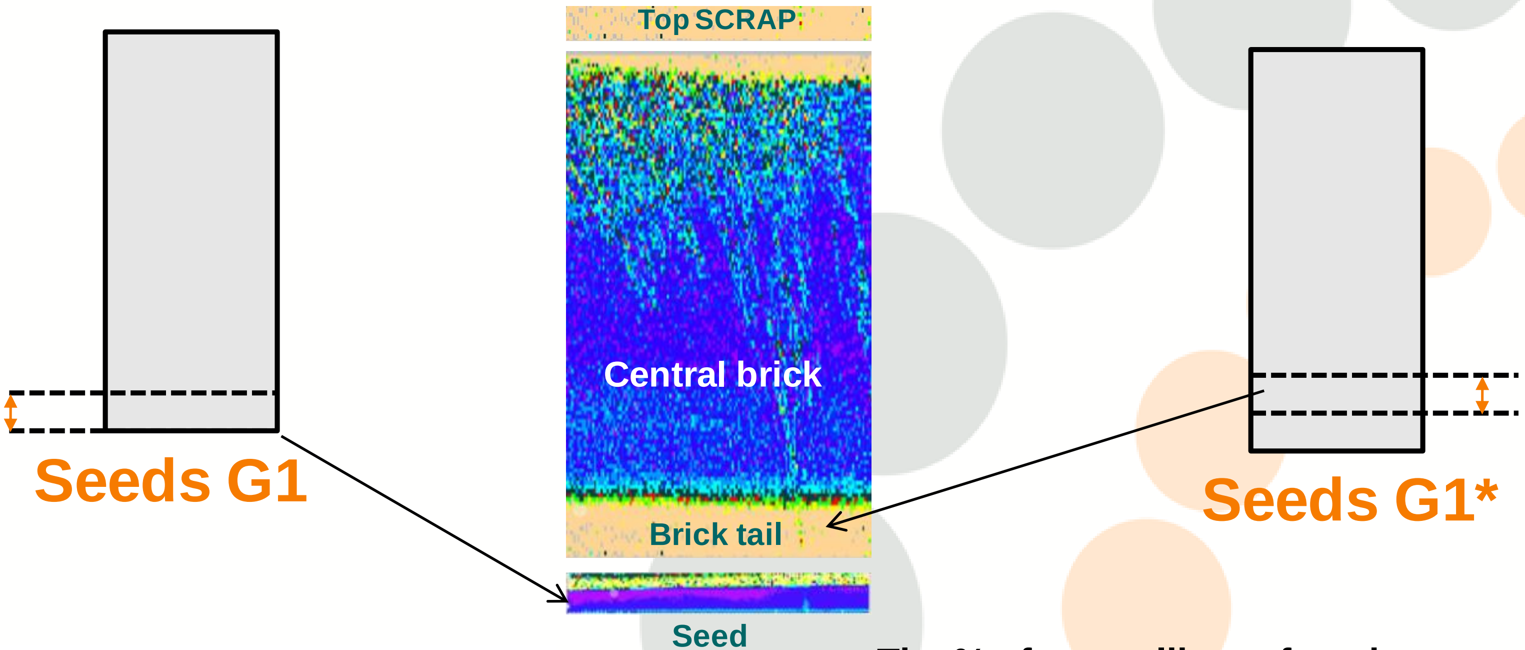
G1

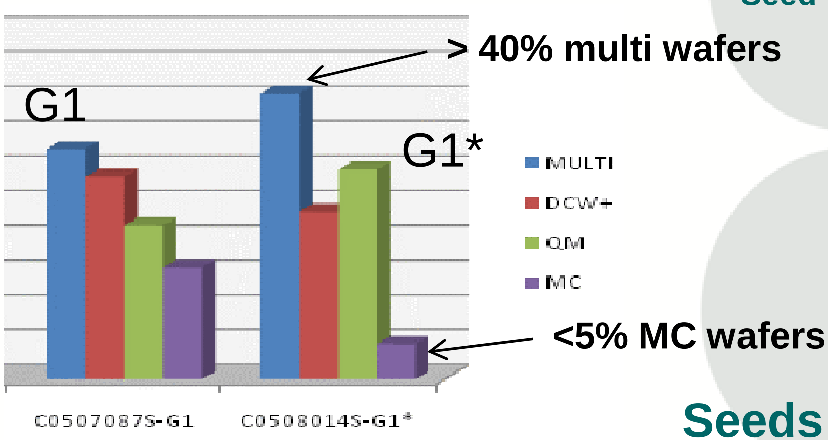
G1*



Photoluminiscence analysis in collaboration with SEMILAB

Manufacturing mono-cast ingots





The % of mono-like wafers decreases from G1 to G1*, but higher average efficiency was observed for G1* based seeds

Impurity effect (interstitial/defects decoration)

Seeds recycling: crystal defects or impurities?

Summary and findings

- High efficiency devices are more and more demanded by the hard and diffuse PV market.

- Quasi-mono based wafers entail one of the most attractive ways of satisfying those demands in a relatively easy and quick way.

- Solar cell/module customers still understanding the overall quasi-mono ingots performance (mono-like regions, average efficiency, even aesthetics…).

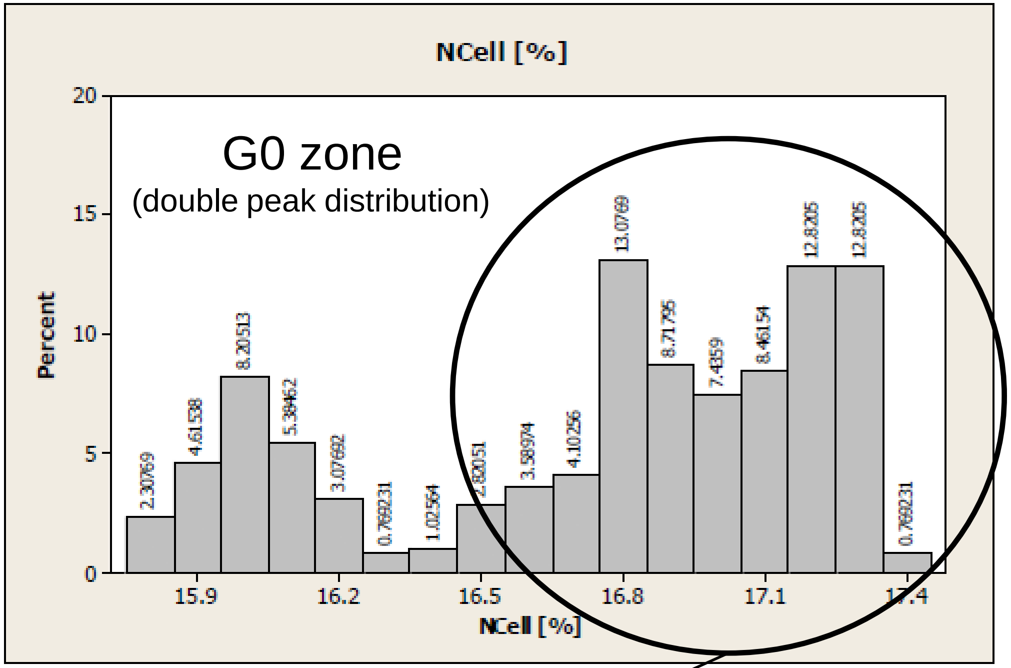
- Mass production are fully dependant on quality and availability of mono seeds and the cost related.

- Recycling of the seeds to reduce costs proven not to be an easy path due to dislocations from thermal stress

Summary and findings

Type of wafer	Isc/A	Voc/mV	Average EFF
G2 zone (ingot 1)	8.26	609	15.85
G0 zone (ingot 1)	**8.45**	**623**	**16.80 (median: 16.90)**
G1 (ingot 2)	8.33	612	16.12
G1* (ingot 3)	8.36	615	16.27

Values corresponding to equivalent samples taken from the respective ingots (DCW+, QM and MC)



Non-optimized iso-texturing process (Isc up to 8.60 A can be reached)

65% of wafers exhibiting >16.80% eff

Current status at DCWafers

- Software and hardware modifications (recipe and furnace hot zone): average efficiency/ingot >17% using iso-texturing process and >17.5% using alkaline-based texturing.

- Study of the origin of the defects when recycling the seed: thermal shock during nucleation, effect of impurities coming from the crucible.

- Avoidance of low efficiency tails. Effect of carbon/oxygen impurities (fine FTIR analysis, LID).

- Use of alternative feedstock with encouraging yield/efficiency results.

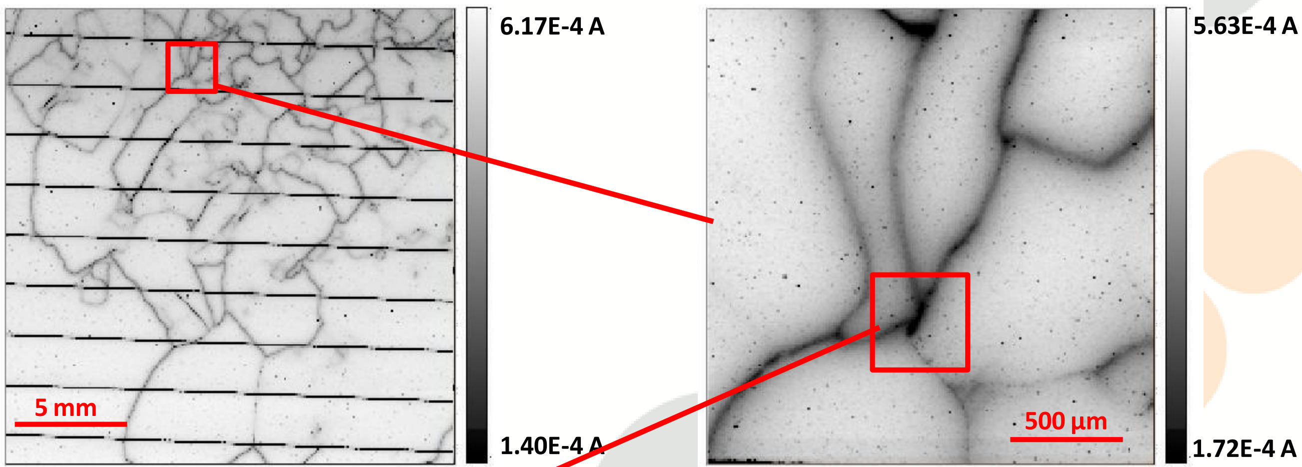
- Cost reduction: increase efficiency by reusing seeds.

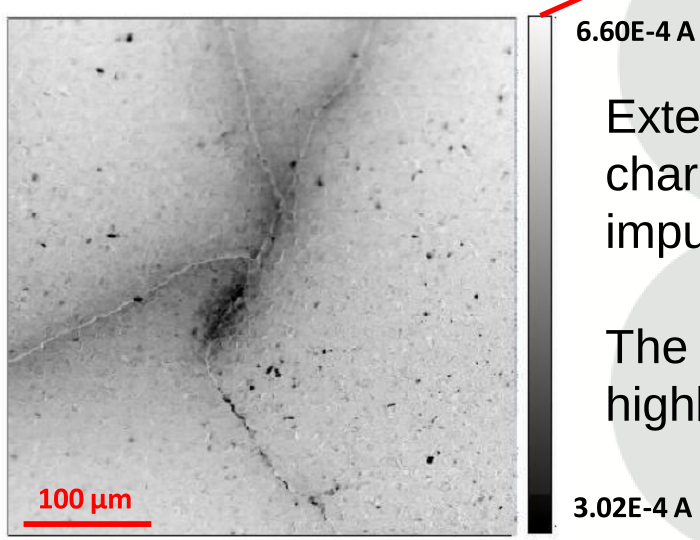
- Development of a pilot scale furnace (70 kg) sharing HEM and DSS features.

Current status at DCWafers

Light Beam Induced Current (LBIC) maps

Defect area (G0-based PV cell)



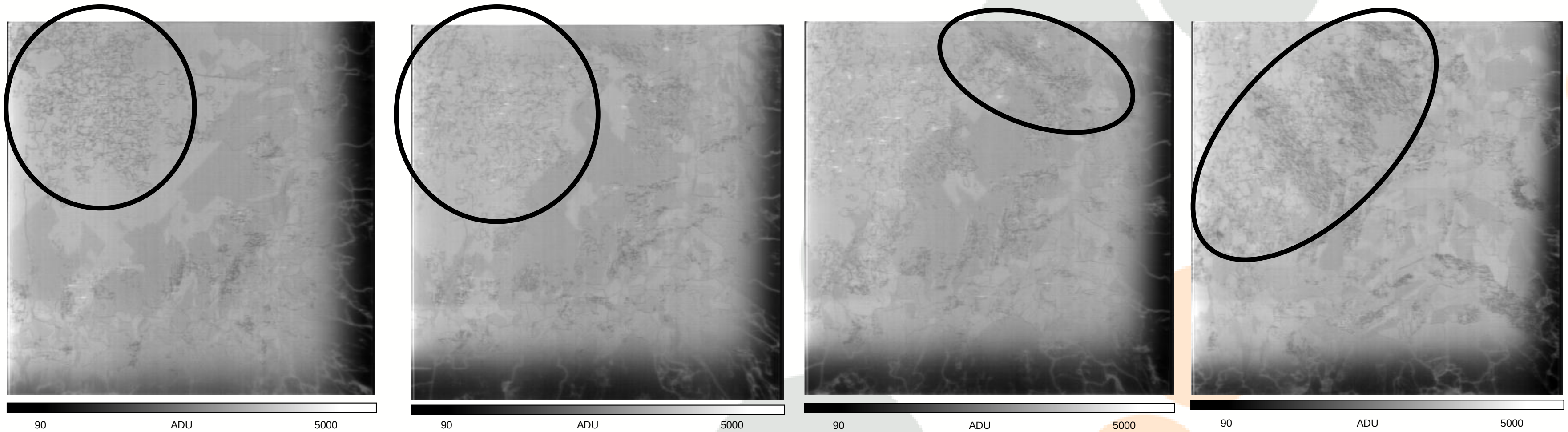


Extended defects with regions exhibiting different charge capture activity (effect of precipitated impurities)

The lower the Isc values the more the density of highly active defects (from G0 wafers to Gn)

Current status at DCWafers

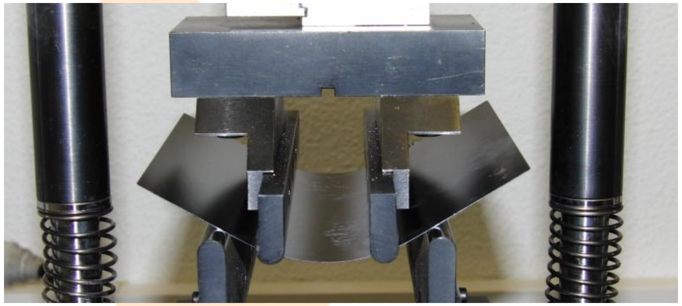
G0 (corner brick)



Top (multi)

Defect density increases from the mono regions and near the mono/multi interfaces

Defect density increase from G0 to Gn seed-based ingots are in agreement with the occurrence of **lower mechanical resistance (fracture tension by FLBT analysis)** (*poster session J. Barredo et al.*)



Photoluminiscence analysis in collaboration with SEMILAB

ACKNOWLEDGEMENTS

GOBIERNO DE ESPAÑA
MINISTERIO DE CIENCIA E INNOVACIÓN

Funds from the Spanish Ministry Of Science and Innovation (MICINN) project nº IPT-420000-2010-22

SEMILAB (Hungary)
Mr. Zoltan Kiss
Mr. Gyorgy Nadudvary
Mr. Nicolas Laurent

cel.celis solar company
Mr. Fernando Suárez
(Spain)

JSPL
Mr. Vijay Krish
(India)

Solland
Dr. Bert Geyer
(Holland)

XGROUP celle e moduli Made in Italy
Dr. Andrea Tomasi
(Italy)

THANK YOU FOR YOU ATTENTION!!

DC Wafers (SPAIN):
Mr. Ismael Guerrero (CTO/General Manager)
iguerrero@dcwafers.com

Dr. Vicente Parra (R&D Manager)
vparra@dcwafers.com